REMARKS/ARGUMENTS

Claim Rejections 35 U.S.C. § 112

Claims 1-6, 10-15 and 25-28 are rejected, under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement. The rejection alleges that the recitation of a "signal from an operating program" in independent Claims 1, 10 and 25 do not have any support in the specification. Applicant respectfully traverses the rejection. For example, in one embodiment of the present invention the specification of the instant application explicitly discloses that "when the sleep function is to be initiated, the operating program sends a first signal to the device under test" (see Instant Application, page 30, paragraph 2). Thus, the amended feature does have support in the specification and withdrawal of the rejection is earnestly solicited.

Claim Rejections 35 U.S.C. § 102

Claims 1-28 are rejected, under 35 U.S.C. §102(e), as being allegedly anticipated by Nemecek et al., U.S. Pat. No. 7,236,921 (hereinafter, Nemecek). Applicant respectfully traverses the rejection in view of the following.

Independent Claim 1 recites a feature whereby upon receiving a first signal from an operating program that indicates that a sleep function is to be performed, initiating the sleep function at the device under test, as claimed.

Independent Claim 1 further recites that in response to said initiating said sleep function, turning off one or more clock of the device under test, as claimed.

In contrast, Nemecek teaches that upon receiving a halt command the clock signals and the data lines are examined (see Nemecek, col. 16, lines 25-30). It is determined that the watchdog timer has expired if the clocks are not functioning and both data lines are asserted high whereas it is determined that the microcontroller is already operating in sleep mode if the clock signals are absent and either data lines is asserted low (see Nemecek, col. 16, lines 30-37). When the microcontroller is in sleep mode the halt command is queued so that the halt command can be implemented at the next opportunity (see Nemecek, col. 16, lines 38-43). When the microcontroller is not asleep, the halt command is queued halting the microcontroller (see Nemecek, col. 16, lines 52-55).

Accordingly, Nemecek teaches that it is determined whether the microcontroller is in sleep mode when a halt command is received. If the microcontroller is in sleep mode, the halt command is queued to halt the microcontroller when the microcontroller wakes. If the microcontroller is not asleep, the halt command is queued and halts the microcontroller. Thus, Nemecek fails to teach or suggest how or when the microcontroller goes into the sleep mode.

Applicant respectfully submits that a halt command, as taught by Nemecek, differs from a first signal indicating a sleep function, as claimed. Moreover, Applicant respectfully submits that determining that the microcontroller is already operating in sleep mode, as taught by Nemecek, fails to teach or suggest how or when the microcontroller goes into sleep mode, thereby failing to teach or suggest receiving a first signal from an operating program that indicates that a sleep operation is to be performed, initiating the sleep function, as claimed. Nemecek fails to teach or suggest a sleep function, as presented and discussed above, thereby failing to either teach or suggest receiving a first signal from an operating program that indicated that a sleep function is to be performed, as claimed.

Furthermore, Nemecek teaches that the watchdog timer expiration causes an internal reset to occur within the microcontroller (see Nemecek, col. 17, lines 2-3). Resetting the microcontroller, as taught by Nemecek, differs from initiating a sleep function, as claimed, because the sleep function does not necessarily reset the microcontroller.

Nemecek further teaches that the watchdog timer expiration causes internal reset in the microcontroller and that the watchdog timer turns off the clocks in the microcontroller (see Nemecek, col. 17, lines 2-4). When no clock signal is detected, the gatekeeper ascertains that a watchdog event has occurred

and causes that gatekeeper crowbars to reset line to a logic high, thereby freezing the state of the microcontroller and the virtual microcontroller, leaving the debug information undisturbed (see Nemecek, col. 17, lines 16-18). Thus, turning off the clocks in the microcontroller in response to detecting a watchdog timer expiration, as taught by Nemecek, fails to either teach or suggest in response to the initiating the sleep function, turning off one or more clock of the device under test, as claimed.

Accordingly, Nemecek fails to anticipate independent Claim 1, under 35 U.S.C. §102(e). Independent Claims 10 and 25 recite features similar to that of independent Claim 1 and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

As per Claim 3, Nemecek teaches that the gatekeeper that is within the base station and is separate from the DUT sends a message informing the host computer of the sleep mode of the microcontroller (see Nemecek, col. 16, lines 38-44 and Figure 8, elements 218, 602 and 232). As such, Nemecek fails to teach or suggest that the first signal is generated by the device under test, as claimed.

As per, Claims 4, 13 and 26, Nemecek teaches that when the microcontroller is in sleep mode, the halt command is queued such that when a

timed event causes the microcontroller to awaken, the microcontroller is halted (see Nemecek, col. 16, lines 38-46). Accordingly, Nemecek teaches that a timed event causes the microcontroller to awaken and halt due to the queued halt command. The rejection interprets "that a timed event has corresponds to a predetermined number of cycles."

Accordingly, the alleged interpretation is that the timed event has a predetermined number of cycles that causes the microcontroller to awaken. Thus, the predetermined number of cycles occurs between when the halt command is received and when the microcontroller awakes, as interpreted by the rejection. Thus, Nemecek fails to teach or suggest determining the number of clock signals received at the emulator device since the second signal was received, as claimed.

Moreover, as discussed and presented above, Nemecek teaches that a timed event causes the microcontroller to awaken and halt due to the queued halt command. Furthermore, as discussed above, the predetermined number of cycles occurs between when the halt command is received and when the microcontroller awakes, as interpreted by the rejection. Thus, Nemecek fails to either teach or suggest resuming execution of the instructions when the determined number of clock signals received at the emulator device since the second signal was received equals a predetermined value, as claimed.

Accordingly, Nemecek fails to anticipate Claims 1-6, 10-15 and 25-28, under 35 U.S.C. §102(e). As such, allowance of Claims 1-6, 10-15 and 25-28 is earnestly solicited.

Independent Claim 7 recites a feature whereby upon receiving the first signal that indicates that a stall function is to be performed, discontinuing sending of the clock signals from the device under test to the emulator device, as claimed. Accordingly, the sending of the clock signals are discontinued when the signal indicates a stall function, but the clock signals may continue to run on the device under test (see Instant Application, page 33, last paragraph).

In contrast, Nemecek teaches that upon receiving a halt command the clock signals and the data lines are examined (see Nemecek, col. 16, lines 25-30). It is determined that the watchdog timer has expired when the clocks are not functioning and both data lines are asserted high (see Nemecek, col. 16, lines 30-37). When the microcontroller is not asleep, the halt command is queued and halts the microcontroller (see Nemecek, col. 16, lines 52-55). Nemecek fails to explicitly teach or suggest discontinuing the sending of the clock signals from the device under test to the emulator device, as claimed.

Moreover, Nemecek teaches that expiration of the watchdog timer causes an internal reset, which causes the watchdog to turn off the clocks (see Nemecek, col. 17, lines 2-4). Turning off the clocks, as taught by Nemecek, differs from discontinuing sending of the clock signals, as claimed. For example, clock signals may be running on a device under test without being sent to an emulator whereas when the clock signals are turned off it is no longer being run on the device under test. Thus, turning off the clocks, as taught by Nemecek, fails to either teach or suggest discontinuing sending of the clock signals, in the claimed fashion.

Accordingly, Nemecek fails to anticipate independent Claim 7, under 35 U.S.C. §102(e). Independent Claims 16 and 21 recite features similar to that of independent Claim 7 and are patentable over Nemecek for similar reasons. Dependent claims are patentable by virtue of their dependency.

As per Claims 9, 19 and 22, Nemecek teaches that halt commands are handled within the base station (see Nemecek, col. 16, lines 55-57). Moreover, Nemecek teaches that expiration of the watchdog timer causes an internal reset to occur within the microcontroller turning off the clocks in the microcontroller (see Nemecek, col. 17, lines 2-4). When the gatekeeper within the base station detects that there is no clocking signals being received it ascertains that a watchdog event has occurred which freezes the state of the microcontroller as

well as the virtual microcontroller to keep the debug information is undisturbed (see Nemecek, col. 17, lines 11-18). Nemecek further teaches rerouting the gatekeeper clock to the virtual microcontroller in place of the normal microcontroller clock (see Nemecek, col. 17, lines 18-20). Accordingly, Nemecek fails to teach or suggest resuming sending of the clock signals from the device under test to the emulator device, as claimed, because Nemecek teaches rerouting the gatekeeper clock such that the clocking signal is received from within the base station.

Accordingly, Nemecek fails to anticipate Claims 7-9 and 16-24, under 35 U.S.C. §102(e). As such, allowance of Claims 7-9 and 16-24 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of rejections under 35 U.S.C. §102(e).

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-28 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-28 overcome the rejections of record and, therefore, allowance of Claims 1-28 is earnestly solicited.

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Respectfully submitted,
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I hereby certify that this correspondence is being electronically transmitted to the USPTO via EFS on the date shown below: December 11, 2007

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